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10/628,562	07/29/2003	Bi-Yun Yeh	SUND 114CIP	4818

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EXAMINER	
RAHMAN, FAHMIDA	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 06/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,562	YEH ET AL.	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/12/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This final action is in response to communications filed on 4/18/2006.

2. Claims 1-10, 12-22, 24-31 have been amended. Claim 11 has been canceled.

Thus, claims 1-10, 12-31 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 4/12/2006 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 7, 9, 12, 15-17, 20, 22, 27 are rejected under 35 U.S.C. 102(e) as anticipated by Klein (US Patent 6216224).

For claim 7, Klein (US Patent 6216224) teaches the following limitations:

A method for accessing initialization data of a central processor unit (lines 55-57 of column 3) **by a ISA-PCI bridge chip** (110) **connected to a bus (112) in a computer system (Fig 1) that also includes a system controller (114) connected between the bus (112) and the central processing unit (106), said method comprising:**

- **accessing said initialization data** (102) **by said ISA-PCI chip (110);**
- **and sending initialization data from said ISA-PCI** (Fig 1 is showing that ROM initialization data is transmitted from 104 to 116 through Bridge 110) **to system controller (114) and thence to central processing unit** (lines 29-32 of column 3)

Klein (US Patent 6216224) does not explicitly mention that 114 is the north bridge and 110 is the south bridge. Instead, 114 is labeled as system controller in line 7 of column 2 and 110 is labeled as ISA-PCI bridge in line 28 of column 4.

It is examiner's position that the system controller and ISA-PCI bridge are known as north bridge and south bridge respectively. To support the statement, Examiner presents Klein (US Patent 5974239), which mentions that system controller is sometimes called the north bridge (lines 47-48 of column 1) and the bridge between PCI and ISA bus is called South bridge (lines 60-61 of column 1; lines 59-60 of column 4). Thus, Klein (US Patent 6216224) interchangeably used "system controller" with "north bridge" and "ISA bridge" with "south bridge".

For claim 9, 104 is the boot ROM, since it contains BIOS.

For claim 12, Klein teaches the following limitations:

A method for accessing initialization data (102 in Fig 1) **for starting a central processor unit** (lines 55-57 of column 3; lines 5-10 of column 1) **in a computer system** (Fig 1) **that also includes a bus (112), an ISA-PCI bridge chip (110) connected to the bus, a non-volatile memory (104) that stores the initialization data (102) and a system controller (114) connected between the bus (112) and the central processing unit (106), the method comprising:**

- **sending a request for the initialization data from the system controller to the ISA-PCI bridge** (lines 25-30 of column 3 mention that the system controller 114 transfers ROM data 102 to RAM 118. Thus, the North Bridge 114 requests for initialization data 102 through South Bridge 110);
- **using the ISA-PCI bridge to access the non-volatile memory and read out initialization data** (Fig 1 shows that the ROM data 102 is read and sent by 110);
- **sending the initialization data from the ISA-PCI bridge to the system controller** (Fig 1 shows the arrow from 104 to 116. Thus, the ROM data 102 is transferred from 104 to 116, which includes sending data from 110 to 114)

- **and activating the central processor unit based on the initialization data received by the north-bridge chip from the south bridge chip** (lines 1-20 of column 2).

Klein (US Patent 6216224) does not explicitly mention that 114 is the north bridge and 110 is the south bridge. Instead, 114 is labeled as system controller in line 7 of column 2 and 110 is labeled as ISA-PCI bridge in line 28 of column 4.

It is examiner's position that the system controller and ISA-PCI bridge are known as north bridge and south bridge respectively. To support the statement, Examiner presents Klein (US Patent 5974239), which mentions that system controller is sometimes called the north bridge (lines 47-48 of column 1) and the bridge between PCI and ISA bus is called South bridge (lines 60-61 of column 1; lines 59-60 of column 4). Thus, Klein (US Patent 6216224) interchangeably used "system controller" with "north bridge" and "ISA bridge" with "south bridge".

For claim 15, 104 is the ROM containing BIOS.

For claim 16, the mentioned steps are required for transferring initialization data from non-volatile memory to system memory through South Bridge under the driving of North Bridge.

For claim 17, note lines 1-17 of column 2.

For claim 20, Klein teaches the following limitations:

a system **for accessing initialization data** (102 in Fig 1) **for starting a central processor unit** (lines 55-57 of column 3; lines 5-10 of column 1), **the system comprising:**

- an ISA-PCI bridge (110);
- **a system controller** (114) **in direct communication with a ISA-PCI bridge** (110) **and the central processor unit** (106);
- **and a non-volatile memory subsystem** (104) **in direct communication with the ISA-PCI bridge storing the initialization data** (102);
- **wherein upon receiving a request from the system controller for obtaining the initialization data** (lines 27 of column 3 mention that the system controller is to transfer the ROM data to RAM. Thus, the North Bridge does the request to obtain ROM data from 104), **the initialization data is accessed by the ISA-PCI bridge** (Fig 1) **and forwarded to the system controller** (lines 1-5 of column 2) **for activating the central processor unit** (lines 1-20 of column 2).

Klein (US Patent 6216224) does not explicitly mention that 114 is the north bridge and 110 is the south bridge. Instead, 114 is labeled as system controller in line 7 of column 2 and 110 is labeled as ISA-PCI bridge in line 28 of column 4.

It is examiner's position that the system controller and ISA-PCI bridge are known as north bridge and south bridge respectively. To support the statement, Examiner presents Klein (US Patent 5974239), which mentions that system controller is sometimes called the north bridge (lines 47-48 of column 1) and the bridge between PCI and ISA bus is called South bridge (lines 60-61 of column 1; lines 59-60 of column 4). Thus, Klein (US Patent 6216224) interchangeably used "system controller" with "north bridge" and "ISA bridge" with "south bridge".

For claim 22, 104 is the ROM containing BIOS.

For claim 27, lines 1-17 of column 2 mention that CPU reads initialization data.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 8, 10, 13-14, 19, 21, 25-26, 28-29 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admission of prior art, in view of Klein (US Patent 6216224).

For claim 1, applicant admits that the following limitations exist in prior art:

A method for accessing initialization data for starting a central processor unit in a computer system (Fig 1 and 2 show that the serial PROM 200 is storing initialization data for starting a central processing unit 208 in a computer system of Fig 1) **comprising:**

- **starting up a north-bridge chip** (line 20 of page 3);
- **requesting said initialization data by said north bridge chip** (lines 20-22 of page 3);
- **receiving said initialization data by said north-bridge chip** (lines 21-22 of page 3).

However, the applicant's admission of prior art does not teach the following limitations:

- **requesting initialization data from a south bridge chip.**

Klein teaches a system where BIOS and initialization data (102) is in a memory 104 connected to South Bridge 110 (Line 28 of column 4 mention that 110 is a PCI-ISA bridge, which is the South Bridge). The memory 104 connected to South Bridge 110 is storing both BIOS and initialization routines (lines 28-33 of column 1 mention that the firmware routines include BIOS and other initialization routines). The north bridge 114 is connected between the central processing unit 106 and a bus 112 (Fig 1). The South bridge chip is connected to the bus 112.

Klein (US Patent 6216224) does not explicitly mention that 114 is the north bridge and 110 is the south bridge. Instead, 114 is labeled as system controller in line 7 of column 2 and 110 is labeled as ISA-PCI bridge in line 28 of column 4.

It is examiner's position that the system controller and ISA-PCI bridge are known as north bridge and south bridge respectively. To support the statement, Examiner presents Klein (US Patent 5974239), which mentions that system controller is sometimes called the north bridge (lines 47-48 of column 1) and the bridge between PCI and ISA bus is called South bridge (lines 60-61 of column 1; lines 59-60 of column 4). Thus, Klein (US Patent 6216224) interchangeably used "system controller" with "north bridge" and "ISA bridge" with "south bridge".

It would have been obvious to one ordinary skill in the art to combine the teachings of Klein and applicant's admission of prior art. One ordinary skill in the art would have been motivated to request initialization data of CPU from a South Bridge chip as disclosed in Klein, since it would make the system compact as only one shared non-volatile memory for BIOS and initialization data is required, which is accessed by CPU through South Bridge.

For claims 2, 3, 8, lines 23-24 of page 2 of applicant's disclosure mention that the initialization data may include SIP data used in AMD CPUs.

For claim 4, note lines 19-21 of [0007] of page 3 of applicant's disclosure, which mention that the South Bridge is powered and starts up the North Bridge.

For claim 5, requesting includes sending a signal from north bridge chip (114) to South bridge chip (104).

For claim 6, lines 22-24 of [0007] of page 3 of applicant's disclosure mention that the CPU sets initial value using initialization data sent by North Bridge and operates normally. Thus, the method further comprises sending said initialization data to the central processor unit of said computer system for starting up the central processor unit.

For claim 10, note lines 19-21 of [0007] of page 3 of applicant's disclosure, which mention that the South Bridge is powered and starts up the North Bridge.

However, applicant's admission of prior art does not mention about accessing initialization data by South Bridge after the North Bridge sends request for initialization data.

Klein teaches that the North Bridge 110 is reading initialization data from South Bridge 104. Thus, the North Bridge passes associated signals to South Bridge.

It would have been obvious for an ordinary skill in the art to combine the teachings of applicant's admission of prior art and Klein. One ordinary skill in the art would have been motivated to send request signal from North Bridge to South Bridge, since North Bridge is closer to CPU and coupled to system memory, where the initialization routines would be transferred. Thus, the North Bridge has to send the signals associated with reading the data to South Bridge.

For claim 13, note lines 19-21 of [0007] of page 3 of applicant's disclosure, which mention that the South Bridge is powered and starts up the North Bridge.

For claim 14, note Fig 1 of applicant's disclosure.

For claims 18, 23 and 30, Klein mentions that the address counter preloads an initial address, which is the highest address for ROM data that is transferred from ROM to RAM in lines 30-35 of column 5. Thus, the ROM data contains an initialization ID.

For claim 19, lines 23-24 of page 2 of applicant's disclosure mention that the initialization data may include SIP data used in AMD CPUs.

For claim 21, Fig 1 of applicant's disclosure show that South Bridge is connected to power supply controller.

For claim 24, Klein mentions that the address counter preloads an initial address, which is the highest address for ROM data that is transferred from ROM to RAM and the initial address may be provided by hardwiring in lines 30-50 of column 5. Thus, ROM includes a predetermined location for storing initialization data. Lines 50-55 of column 1 mention that after the CPU initialization is executed, it can be discarded and the RAM contains remaining BIOS. Thus, the initialization routines and BIOS have to be stored in separate area because they are separate routines.

For claim 25, lines 23-24 of page 2 of applicant's disclosure mention that the initialization data may include SIP data used in AMD CPUs.

For claim 26, Klein is retrieving the initialization data by the south bridge chip; and sending the initialization data to the north bridge chip.

However the south bridge chip of Klein does not include means for: activating the north bridge chip. Applicant's admission of prior art activates North Bridge by South Bridge.

It would have been obvious to one ordinary skill in the art to have combined the teachings of applicant's admission of prior art and Klein. One ordinary skill in the art would have been motivated to activate the North Bridge by South Bridge as disclosed in applicant's admission of prior art, since South Bridge contains the initialization data, which should be started before other components.

For claim 28, applicant's admission of prior art teaches the following limitations:

a method for accessing initialization data for starting a central processor unit in a computer system (Fig 1 and 2 show that the serial PROM 200 is storing initialization data for starting a central processing unit 208 in a computer system of Fig 1), **the method comprising:**

- **activating a south bridge chip by a power supplier controller** (lines 17-18 of [0007] of page 3 mention that the South Bridge is powered when the system is powered on. Fig 1 shows that the South Bridge is connected to power supply controller. Thus, the South Bridge chip is activated by by the power supply controller);
- **activating a north bridge chip by the activated south bridge chip** (lines 19-22 of [0007] of page 3 mention that the South Bridge sends a signal to start North bridge); requesting to access the initialization data (lines 20-23 of [0007] of page 3 mention that the North bridge sends request to access initialization data);
- **accessing the initialization data stored in a non-volatile memory** (200 of Fig 2 contains initialization data, which is a Non-volatile memory);
- **sending the initialization data to the north bridge chip** (Lines 21-23 of [0007] of page 3 mention that the North bridge receives initialization data);
- **sending an initialization signal to the central processor unit by the north bridge chip upon receiving the initialization data** (lines 20-25 of [0007] of page 3 mention that CPU uses initialization data sent by North Bridge);

- **and activating the central processor unit by the initialization signal** (lines 23-25 of [0007] of page 3 mention that the CPU operates normally after setting initial values).

Applicant's admission of Prior Art does not teach the following limitations of claim 28:

- Requesting South Bridge chip for initialization data
- Accessing initialization data by South Bridge
- Sending initialization data by South Bridge

The system of Klein teaches that the non-volatile ROM containing initialization data 102 is transferred to RAM under the driving of North Bridge through South Bridge 110. For that, the usual procedures have to include requesting for initialization data through South Bridge, accessing initialization data by South Bridge and sending initialization data by South Bridge.

Klein (US Patent 6216224) does not explicitly mention that 114 is the north bridge and 110 is the south bridge. Instead, 114 is labeled as system controller in line 7 of column 2 and 110 is labeled as ISA-PCI bridge in line 28 of column 4.

It is examiner's position that the system controller and ISA-PCI bridge are known as north bridge and south bridge respectively. To support the statement, Examiner presents Klein (US Patent 5974239), which mentions that system controller is

sometimes called the north bridge (lines 47-48 of column 1) and the bridge between PCI and ISA bus is called South bridge (lines 60-61 of column 1; lines 59-60 of column 4). Thus, Klein (US Patent 6216224) interchangeably used "system controller" with "north bridge" and "ISA bridge" with "south bridge".

It would have been obvious to one ordinary skill in the art to combine the teachings of Klein and applicant's admission of prior art. One ordinary skill in the art would have been motivated to request initialization data of CPU from a South Bridge chip as disclosed in Klein, since it would make the system compact as only one shared non-volatile memory for BIOS and initialization data is required, which is accessed by CPU through South Bridge.

For claim 29, 104 of Klein is a non-volatile memory containing BIOS.

For claims 31, lines 23-24 of page 2 of applicant's disclosure mention that the initialization data may include SIP data used in AMD CPUs.

Response to Arguments

Applicant's arguments filed on 4/12/2006 have been fully considered but they are not persuasive.

Regarding claims 7, 20 and 28, applicant argues that Klein does not teach using a south bridge chip to access initialization data and then sending the initialization data from south bridge to north bridge and then to CPU.

Examiner disagrees. It is examiner's position that the system controller and ISA-PCI bridge are known as north bridge and south bridge respectively. To support the statement, Examiner presents Klein (US Patent 5974239), which mentions that system controller is sometimes called the north bridge (lines 47-48 of column 1) and the bridge between PCI and ISA bus is called South bridge (lines 60-61 of column 1; lines 59-60 of column 4). Thus, Klein (US Patent 6216224) interchangeably used "system controller" with "north bridge" and "ISA bridge" with south bridge. Fig 1 of Klein (US Patent 6216224) shows that 110 accessed initialization data in 102 to send it to north bridge 114. Lines 29-31 of column 3 mention that CPU fetches ROM data. Thus, the initialization data is reached to the CPU from system controller or north bridge.

Regarding claims 1, 12, 20 and 28, applicant argues that Klein does not teach sending request for initialization data to a south bridge chip from North bridge chip.

Examiner disagrees. Lines 3-8 of column 2 mention that CPU drives the system controller to transfer ROM data to RAM. Thus, system controller drives the transfer process, which must include sending a notion (or, request) to ROM that the ROM needs to be transferred to RAM. The ROM cannot be accessed by system controller without

accessing ISA bridge first as shown in Fig 1. Thus, the request for ROM data from system controller to ISA bridge is in the system of Klein. The initialization data is accessed for activating the CPU as mentioned in lines 20-35 of column 3 of Klein (CPU is in reset state while system controller transfers ROM data to RAM. CPU is activated to fetch ROM data from RAM after the transfer is complete).

Regarding the motivation behind combining AAPA and Klein, applicant argues that ordinary skill in the art would reject the notion of involving a south bridge chip in initialization of a CPU on the ground that this would surely slow down the initialization.

Examiner disagrees. The ROM of Klein not only stores initialization routines but also BIOS and POST (lines 28-33 of column 1). AAPA admitted that a conventional PC stores BIOS in ROM that is connected to South-bridge (lines 29-45 of column 1). In such a case, ordinary skill in the art would be very much motivated to store all the initialization data and routines with BIOS in the ROM, since that would reduce the need for multiple ROM.

Regarding claims 1 and 28, applicant argues that AAPA does not teach sending a request North bridge chip as generating clock like signal is different from sending request.

Examiner disagrees. Both AAPA and Klein teach sending request by North bridge. Without a request or notion, the non-volatile ROM can't be accessed. Lines 3-8 of column 2 of Klein mention that CPU drives the system controller to transfer ROM data to RAM. Thus, system controller drives the transfer process, which must include sending a notion (or, request) to ROM that the ROM needs to be transferred to RAM. Claim does not require the shape of request signal. Thus, any signal that carries the message that the ROM needs to be accessed for initialization data is a request. Both Klein and AAPA teach such request as both are accessing the ROM that contains the initialization data. Such request has to follow the 114-112-110-108-104 as it is the only single path and includes north bridge, south bridge.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fahmida Rahman
Examiner
Art Unit 2116

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